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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/695,335

10/28/2003

Jeffrey P. Gambino

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09/27/2004

IBM MICROELECTRONICS
INTELLECTUAL PROPERTY LAW
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EXAMINER

RAO, SHRINIVAS H

ART UNIT

PAPER NUMBER

2814

DATE MAILED: 09/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/695,335	GAMBINO ET AL.	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 December 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 13-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☐ Claim(s) 13-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>10/28/2003</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Priority

Receipt is acknowledged of paper submitted under 35 U.S.C. 1120 claiming priority from U.S. Serial No. 09/ 965,288 filed on September 27, 2001 which papers have been placed of record in the file.

Divisional Prosecution Application

The request filed on 10/28/2003 for a Divisional Prosecution Application (DA) under 37 CFR 1.53(d) based on parent Application No. 09/965,288 is acceptable and a DA has been established. An action on the DA follows.

Information Disclosure Statement

Acknowledgment is made of receipt of Applicant's Information Disclosure Statement (PTO-1449) filed 10/28/2003.

The references on PTO 1499 submitted on 10/28/2003 are acknowledged. All the cited references have been considered.

However the foreign patents and documents cited by applicant are considered to the extent that could be understood from the abstract and drawings.

Preliminary Amendment Status

Acknowledgment is made of receipt of Applicant's Preliminary amendment filed on 10/28/2003.

Therefore claims 13-20 as recited in the preliminary amendment are currently pending in the Application.

Claims 1-12 have been cancelled by the preliminary amendment.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 13-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Augusto (U.S. Patent No. 5,963,800 herein after Augusto) .

With respect to claim 13 Augusto describes a thin film insulating (Fm) metal oxide semiconductor field effect transistor (MOSFET) comprising: a bottom Si-containing layer, (Augusto col. 10 lines 3-5) an insulating region present atop said bottom Si-containing layer, (augusto fig. 3 # 5,7 col. 11 lines 29-46) said insulating region having at least one partial opening therein; (Augusto figure 3 # 5) a gate region formed in said partial opening, (agosto fig. 3 # 13) said gate region comprising two regions of gate conductor that are separated from channel regions by an insulating film, (Augusto fig. 3 # 13 separated from 3 by 11) said insulating film having opposite vertical surfaces adjacent to the channel regions; (Augusto figure 3 # 11) source/drain diffusion regions abutting said gate region, (Augusto figure 3 # 5',7' (source) and #1' (drain) abutting gate 13) said source/drain diffusion regions having junctions that are self-aligned to the channels regions as well as the gate region; (Augusto figure 3 #

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5', 7' (source) and #1' (drain) self-aligned with channel 3, 3') and insulating spacers that separate the gate region and the source/drain diffusion region formed orthogonal to said insulating film. (Augusto figure 3 spacer not numbered orthogonal to gates 13).

With respect to claim 14 Augusto describes the Fm MOSFET of Claim 13 wherein said insulating region includes an insulating layer of an SOI material. (Augusto col. 25 lines 65-66).

With respect to claim 15 Augusto describes the Fm MOSFET of Claim 13 wherein said partial opening exposes a portion of said insulating layer of said SOI material. (Augusto figures 9.4, 15.1, etc.)

With respect to claim 16 Augusto describes the Fm MOSFET of Claim 13 wherein said insulating film is formed surrounding a portion of a Si-containing layer, said insulating film is comprised of a gate dielectric. (Augusto figure 9.4, 15.1 insulators on sides)

With respect to claim 17 Augusto describes the Fm MOSFET of Claim 16 wherein said gate dielectric is comprised of an oxide, a nitride, an oxy nitride or any combination or multi layer thereof. (Augusto figure 15.1, col. 27 lines 5-65).

With respect to claim 18 Augusto describes the Fm MOSFET of Claim 13 wherein said regions of gate conductor are each comprised of polysilicon, amorphous Si, a conductive elemental metal, an alloy of a conductive elemental metal, a nitride or silicide of a conductive elemental metal or multi layers thereof. (Augusto col. 6 line 50 and PMOS or NMOS by definition is a metal gate)


With respect to claim 19 Augusto describes the Fm MOSFET of Claim 13 further comprising silicide regions formed atop said source/drain diffusion regions. (Augusto col. 6 line 50).

With respect to claim 20 Augusto describes the Fm MOSFET of Claim 13 wherein said source/drain diffusion regions are formed in a portion of a patterned Si-containing layer. (Augusto figure 7 (s) and (d) formed in patterned Si containing layer).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (571) 272-1718. The examiner can normally be reached on 8.00 to 5.00.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Steven H. Rao

Patent Examiner

September 22, 2004.



LONG PHAM
PRIMARY EXAMINER